

Guest Editors' Introduction: Big Innovations in Small Packages

Bruce C. Kim

University of Alabama

Yervant Zorian

Virage Logic

■ **CONVENTIONAL** single-die microelectronic packages on a printed circuit board have been with us for a long time. These electronic packages provide a means of interconnecting, powering, cooling, and protecting integrated circuit chips. Today, system in package (SiP) provides a variety of packaging requirements for computer, consumer, aerospace, military, and medical electronic applications by stacking individual IC chips to form 3D circuits. This packaging technology offers reduced form factor to enhance high performance and reliability.

SiP evolution

Electronic packaging is an integral part of computer systems design. The most well-known packaging technology is a multichip module (MCM), which integrates multiple known good dies (KGD) on a high-density substrate. In the 1980s and 1990s, MCM packaging was used for high-end computer systems. However, MCM was a 2D packaging implementation that did not go too far for various reasons. In the mid-1990s, the industry moved to stacking IC chips for creating high-density 3D circuits. This extension of MCM, SiP, became a well-known technology for reducing form factor and is now the fastest-growing microelectronics packaging technology in the semiconductor industry.

SiP design and test is a viable, rapid, and cost-effective solution to high-density system integration in a single package. Today's SiP technology involves the system integration of multiple dies from various technologies into a common package—for example, integrating digital logic, flash memory, DRAM, analog, and RF functional blocks on a single SiP to meet the needs of today's small, low-cost consumer products. This system integration could reduce form factor, improve perfor-

mance, accelerate time to market, and reduce power consumption.

Challenges

Although SiP technology promises enormous benefits over conventional packaging technology, it faces several challenges. The most critical issues are design and test methods and solutions. Design automation methodologies for rapid deployment in SiPs and test technologies for SiPs are required to produce SiP products in a timely manner. In the accelerated time-to-market business world, we noted several immediate challenges. First, common EDA tools are necessary for integrating mixed-signal and RF IC chips. SiPs contain digital, mixed-signal, and RF functional blocks. EDA tools for design and analysis should be available to realize SiPs with a variety of technologies. A prime example is signal integrity; EDA tools should address electrical and thermal modeling of SiPs. Second, KGD should be readily available for SiP designers. One MCM bottleneck was KGD availability. Lack of KGD in digital, mixed-signal, and RF functional blocks will delay further developments in SiP for complete system integration. Finally, the most challenging part of SiP's survival is the proliferation of integrated passive devices at the SiP substrate level. To integrate mixed-signal and RF blocks into a SiP, the SiP vendors must introduce massive amounts of integrated passive devices (IPD) into the SiP substrates. This challenge involves fabricating and modeling technological breakthroughs. The National Electronics Manufacturing Initiative roadmap lists integrated passives in SiP as one of the fastest-growing markets in packaging technology.

The special issue

This special issue on SiP design and test provides a wide perspective from academia and industry and a complete overview of SiP design and test.

Package technology is an essential part of electronics system design. Rickert and Krenik describe the trade-offs between SiP, package-on-package (PoP), and system-on-chip (SoC). During the design cycle, package design engineers must decide on packaging to ensure smooth integration into the final product. This article provides case studies on packaging technologies to reduce cost and time to market for mobile phone applications.

Design engineers are challenged with two separate entities: chip design and package design. Because a SiP is an integration of multiple dies into one package, engineers need a tool to combine the two entities easily and execute them concurrently. Brandtner demonstrates a seven-die SiP design that implements a chip-and-package codesign platform using available EDA tools.

The issue next addresses SiP's testing aspects. SiP integrates multiple dies in a common package. A SiP's test flow differs from SoC test because SiP integrates parts from multiple vendors. This is a growing problem in the SiP design-and-test community that requires a new test strategy and corresponding flow. Appello et al. provide test strategies for KGD and known good substrates in the SiP. Their article proposes a new paradigm for testing a SiP using the IEEE 1500 standard for embedded cores on SiP.

A SiP's highly integrated packaging typically has high-performance characteristics. Many SiP packages contain low-cost 3D stacked chips interconnected by fine wire bonds. In a high-frequency spectrum, these wire bonds can cause discontinuities resulting in signal degradation. Kam et al. provide a low-cost solution to problems associated with wire bonding in high-frequency SiP packages and propose new design methodologies to reduce these discontinuities. In their article, they describe design rules for discontinuity cancellation in the signal paths and low-inductance return paths on the package.

Integrating multicore heterogeneous systems into a single SiP has challenged many design-and-test engineers. Overcoming these obstacles requires a common integration tool for digital, analog, RF, and thermal designs. Madisetti proposes a platform-centric design methodology for modern systems that use SiP, SoC, and system-on-package (SoP) technologies.

Our final set of authors, Kerzerho et al., describes a

new and practical test methodology for data converters embedded in SiP. The authors present a novel design-for-testability technique to test a set of embedded ADC and DAC designs in a complex SiP. The technique provides fully digital testing on the converters, which significantly reduces testing costs.

SYSTEM IN PACKAGE'S SUCCESS depends on overcoming the many challenges that we described, including those in this special issue. We hope that these articles will help you to design and test system-in-package products. ■



Bruce C. Kim is an associate professor in the Department of Electrical and Computer Engineering at the University of Alabama, Tuscaloosa. He received his PhD in electrical engineering from Georgia Institute of Technology. He has received the National Science Foundation Career Award, as well as the Meritorious Service and Outstanding Contribution awards from the IEEE Computer Society. Kim serves as the chair of the Technical Committee on Electrical Test with the IEEE Components, Packaging, and Manufacturing Technology Society. He is a Golden Core member of the IEEE Computer Society, a senior member of the IEEE, and a senior member of the International Microelectronics and Packaging Society.



Yervant Zorian is vice president and chief scientist of Virage Logic. He previously was the chief technology adviser of LogicVision and a Distinguished Member of Technical Staff at Bell Labs. Zorian received his PhD in electrical engineering from McGill University and his executive MBA from the Wharton School of Business, University of Pennsylvania. He is the IEEE Computer Society vice president for conferences and tutorials, the founder and chair of the IEEE 1500 Working Group, and a Fellow of the IEEE.

■ Direct questions and comments about this special issue to Bruce C. Kim, Electrical and Computer Engineering Dept., University of Alabama, 317 Houser Hall, Tuscaloosa, AL 35487; bruce.kim@ieee.org.